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A four-side-buttable tiling scheme for a near real-time digital radiography detector for medical applications

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Abstract
A four-side- buttable tiling scheme to smaller size CMOS imagers or tiles has been proposed for simpler fabrication of a large area digital radiography detector with higher yields. The detector can be operated in the low resolution mode (fluoroscopy) and high resolution mode (radiography). Each CMOS imager pixel uses an N-well to P- substrate photodiode to integrate photo-generated charge and employs a thin oxide capacitor in parallel with the photodiode to increase the maximum charge handling capacity of the pixel. The signal charge is read out to a common signal line using two series connected NMOS transistors which are controlled by row and column scanning registers integrated on the imager array. In this scheme, all the devices (i.e. photodiodes, transistors) and read-out electronics are made using single crystal silicon and the read-out electronics are buried underneath sensing areas.

I. INTRODUCTION

Traditional radiography uses a silver halide photosensitive film and an intensifying screen (or phosphor) in a cassette to capture latent image which is subsequently developed to form visible images which can be displayed on a light box for diagnosis and kept as an archival record. In the late 70's and early 80's, digital imaging modalities , such as computed tomography, ultrasound, nuclear medicine, magnetic resonance imaging, and digital subtraction angiography had moved the trend further toward digital imaging. However, one of the missing link in the digital imaging network for enhancing the quality and productivity of the radiology departments was the digital radiography or DR system. Realizing this critical issue, in 1987, we were asked by the upper managers of 3M Company to look into a digital radiography detector which can replace the conventional x-rays film-screens which are heavy to carry, long time to image and require large storage space. Special features of the new x-ray imaging capture are: large area, flat panel, near-real time imaging, solid state detectors with electronic readout mechanisms, advances in display and computer-aided diagnosis, archiving and communication. We started to work first with the indirect imaging type, that is phosphor/amorphous silicon photodiodes (a-Si PDs) /a-Si thin film transistors (a-Si TFT's); where X-rays were converted into light though a layer of phosphor, to be sensed by PDs and the signal was sent out to the peripheral circuitry, by turning on TFT's [1]. We then came up with the direct imaging type in 1989, that consisted of a thick amorphous selenium photoconductor (a_Se PC)/ a-Si thin film transistors; in this structure charges were generated in a thick a-Se PC and the signal was read out by opening TFT's [2-4]. The read-out electronics at the periphery were made from single crystal silicon (c-Si). The issues facing us at that time was the yield in producing large area panels with millions of pixels. Therefore, we developed the so-called" tiling approach" where a multitude of x-rays sensing modules consisting mainly of a-Si PDs/a-Si TFT's (indirect type) and mainly a-Se PC/a-Si TFT's (for direct type) were juxtaposed in an assembly on a large common glass substrate wherein at least one precision-ground edge and at most three edges formed abutment with edges of another modules; and the readout electronics were built around the module assembly with discrete modules to maintain good manufacturing yields. A common phosphor or a continuous photoconductor/dielectric layers were disposed over the plurality of juxtaposed modules for the indirect and direct type sensing panels, respectively. We had successfully developed prototypes and then products of digital radiography detectors for chest imaging and mammography. The rest is history: we were lucky to be among the firsts in this exciting field ; DR x-rays imaging systems of both direct and indirect types have been available in many hospitals worldwide, especially in the area of digital mammography.

In this report, we will present an extended tiling approach to smaller size CMOS imagers or tiles; this time, all the devices (photodiodes, transistors) and read-out electronics were made using single crystal silicon (c_Si) and the read-out electronics are buried underneath sensing areas . We call this approach the four-side-buttable tiling scheme. The main objective of this approach is for simpler fabrication of DR detector with higher yields and high image quality [5-7] for a large size panels (17" x17" for chest and 8" x 10" for mammography). Pixel size is 85 microns square

for an X-ray exposure range of 0.01 mR to 100 mR. The design can be applied to both direct type and indirect type digital radiography.

II. CONSTRUCTION OF THE DETECTOR

The proposed tilling approach looks promising but encounter several technical issues, nevertheless: (i) busses and circuitry make the pixel crowded and interfere with photon detection for a high fill factor; (ii) a technique is required to combine small silicon chips into a large detector array and (iii) how to bring out signals from the individual tiles without introducing dead spaces. To solve problem (i) a wafer thinning technology had been developed for small c-Si visible imagers, which have been bonded to a thin glass substrate for mechanical stability, giving a high fill factor for each pixel. To solve problem (iii), a novel circuit design was devised, in which all the read-out and selection circuitry were distributed throughout the array. No extra read-out spaces were required on the periphery of the sensor. For bonding/packaging in (ii), we employed the existing flip-chip to provide a path to manufacture a complete DR detector.

Basic structure of the pixel element 10 is shown in Fig. 1.

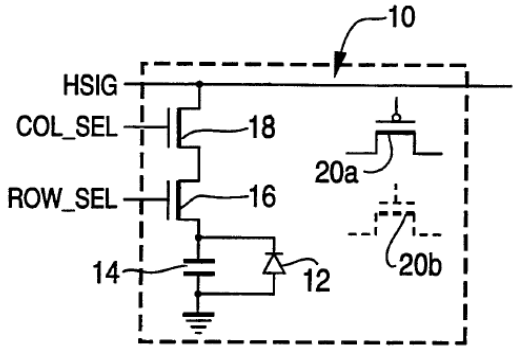

Fig.1. Structure of a pixel element.

In Fig.1, photodetector (phototransducer) 12 is implemented using an N-well to P substrate photodetector to integrate photo-generated charge . The photodetector is coupled in parallel with a capacitor 14 to increase the maximum charge handling capacity of pixel element. The photodetector includes an N well 40 in a P substrate 42. A 1 pF Tox capacitor 14 is set in parallel with the photodetector, as shown in Fig.2. Series connected transistors 16 and 18 couple between photodetector and a signal line (HSIG) and are responsive to the row select line (ROW_SEL) and column select line (COL_SEL), respectively. When these series connected transistors/or switching transistors (both are NMOS in this example) are activated, the charge of pixel element is read out to HSIG. In addition to series connected transistors, one or more "configurable" transistors 20a (independent of the series connected transistors) and optional transistors 20b are included in the pixel element. The extra transistors or "configurable" transistors , along with similar extra transistors within each of the remaining pixel elements in the pixel array, are "configured" with polysilicon and/or metallization interconnections as necessary to form the circuitry needed to implement desirable functions. These functions may be, for example, signal line source followers, analog switches, row and column scanning registers and sense amplifiers. These transistors may be NMOS or PMOS or a mixture of the two types.

Because the peripheral functions are spread over many pixel elements on a pixel array, area at the edges of the pixel array is not needed for the above peripheral functions as in the case of conventional imager designs. This configuration allows the pixel array to have a very small dead space at the edges. Accordingly, multiple imager arrays may be joined along the edges to form larger arrays. Any distortion caused by the small gaps at the joined edges may be corrected using image processing techniques. The result is a "seamless" overall imager array using multiple component four-side- buttable pixel arrays. Since each components array is made separately at a smaller area, the manufacturing yield of the matrix of component arrays is much larger than for an equivalent monolithic array.

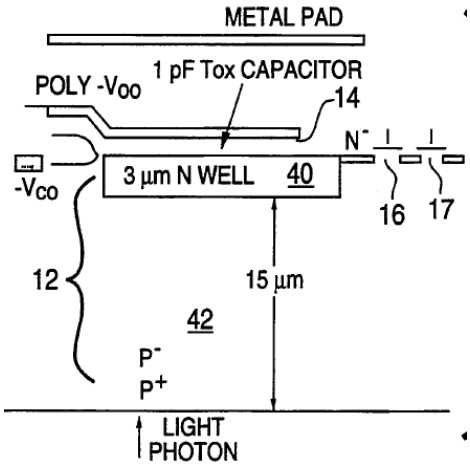

Fig.2. Layouts for the basic components of a pixel element.

Fig. 3 shows a schematic representation of three pairs of pixel elements having their respective extra transistors configured for three different functions.

For purposes of clarity, only one pixel element from each pair is described below. Pixel element 210 is configured to reset function. The pixel element includes a photodetector 212 with parallel capacitor 214. Series connected transistors 216 and 218 are coupled between

photodetector and the horizontal signal line (HSIG). The respective gates of the series connected are coupled to the ROW-SEL line and the COL-SEL line such that when both select lines are active, the charge of pixel element (held by capacitor connected in parallel) is read out onto HSIG, similar to the device operation in Fig.1.

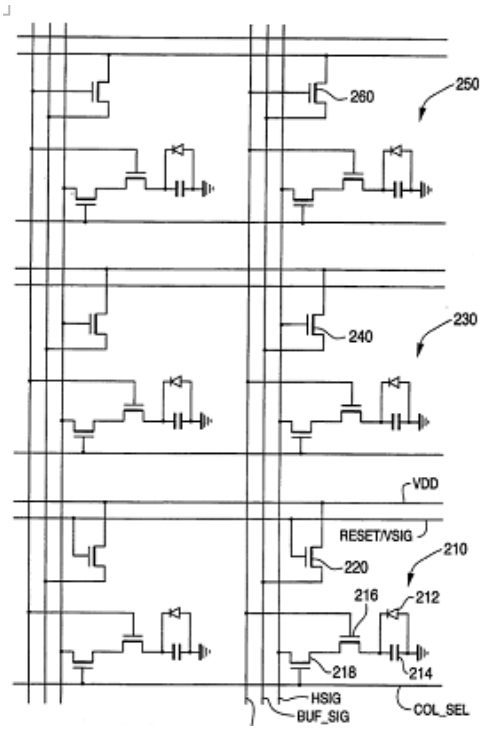

Fig.3 : A schematic representation of three pairs of pixel elements with configured transistors.

In general, the configuration of the photodetector, capacitor and the two switching transistors are the same for each pixel element, however, it is the configuration of the extra transistors 220, 240 or 260 which changes, thereby allowing peripheral circuitry to be implemented within the pixel arrays.

In 210, to implement the reset function, the extra transistor 220 is coupled between a signal line which conveys a source of reference potential (e.g. VDD) and HSIG such that when the RESET/VSIG line is activated (gate) and the pixel element 210 is selected, and reset.

This resetting of pixel element is accomplished by charging the capacitor to VDD with respect to ground potential. During the imaging process, when the photodiode 212 is illuminated, it will reduce the level of charge on the capacitor, reducing the potential with respect to ground.

The extra transistor 240 of pixel element 230 is configured to implement the amplifier function. Drain and source electrodes of transistor the extra transistor are connected to the signal lines VDD and BUF-SIG signal lines, respectively, while its gate electrode is connected to the signal line HSIG . In this configuration, the signal on HSIG (when HSIG is active) modulates the conductivity of the transistor, which effectively causes it to act as an amplifier. In this instance, an amplified version of the signal on HSIG (i.e., a signal having the same characteristics as HSIG) is placed on the BUF- SIG line. In other words, placing a buffered (i.e., amplified) version of the signal on the HSIG line onto the BUF-SIG line.

The layout of pixel element 250 is basically the same as that of pixel elements 210 and 230. The only significant difference is how the extra transistor 260 is interconnected. In said pixel element, the source and drain electrodes of transistor 260 are connected between the signal lines RESET/VSIG and BUF-SIG and the gate electrode is connected to the ROW-SEL to implement the analog switch function. In this configuration , the signal on the ROW-SEL signal line turns on transistor 260 which effectively acts as a switch by routing the signal on the BUF-SIG line onto the REST/VSIG line from which it can then be read.

In addition to the above configuration of the extra transistors, it is also desirable to be able to implement an inverter device available, for example, to simplify the implementation of scanning circuits. For example, the extra transistors can be coupled to implement a CMOS inverter circuit, where an input signal applied to the IN line produces an inverted version of the signal on the OUT line. Fig. 4-a shows a layout for use with reset function in Fig. 3 (as shown in Fig. 4-b). In this figure, the outline of photodetector 212 includes a tab-line extension which connects with transistor 216. Transistor 216, in turn, is connected in series with transistor 218. As shown, the ROW-SEL and COL-SEL lines are connected to the gates of transistors 216 and 218 for controlling access to the state of photodetector and capacitor (i.e. the amount of electrical charge on the capacitor). The extra transistor 220 is connected between the VDD and HSIG signal lines with its gate connected to RESET/-VSIG line, and the transistors 216 and 218 are rendered conductive by the COL-SEL and ROW-SEL signal, the element 220 is reset.

III. LOW RESOLUTION VS HIGH RESOLUTION

The field of medical imaging includes fluoroscopic imaging (dynamic) and radiographic imaging (static). In radiographic imaging, very high resolution read-out is desired. In contrast, for fluoroscopic imaging, the image may be read-out in a lower resolution mode, although it is desirable to obtain an image read-out within a fast period of time. The consolidation of a low resolution and high resolution system into a single medical imaging device provides an economical and convenient, multifaceted imaging device in a single unit. In this device construction, the pixel array switch means are responsive to a low

resolution input signal and include an output signal line. The switch means also include a transistor. First means for

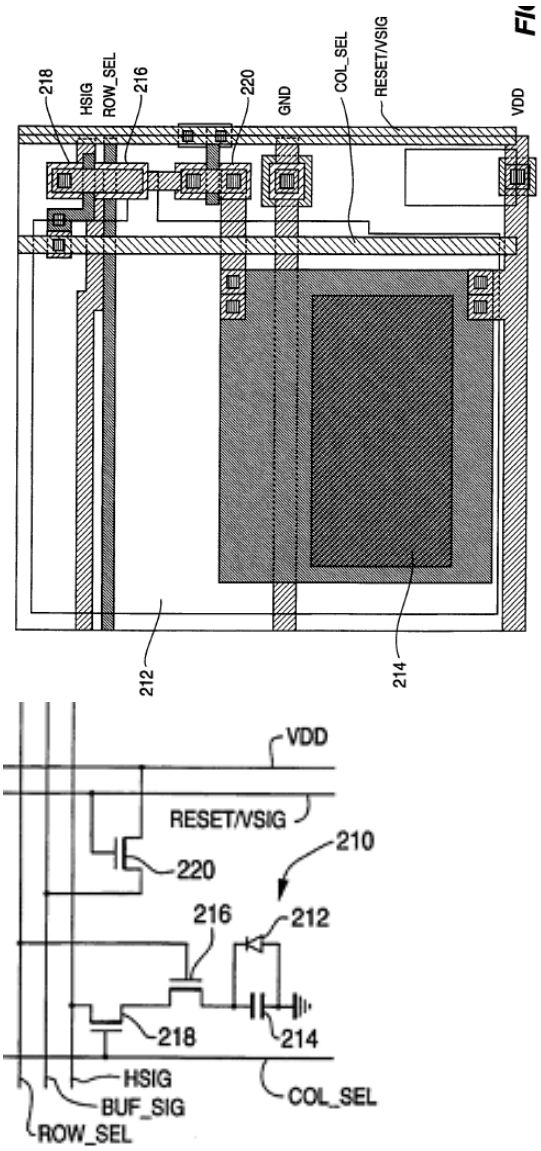

Fig. 4: A layout of pixel element 210 suitable for use with reset function.

buffering signals is coupled between the first signal line and the output signal line. The first means for buffering signals may include a transistor configured as a source follower, and the second means for buffering signals may include a transistor configured as a source follower. The pixel array further comprises means for selectively outputting the buffered output signals to an imaging device. The means for selectively outputting the buffered output signals includes a multiplexer. The pixel array further includes means coupled to the first signal line and the second signal line for resetting the first signal line and the second signal line.

The resolution of the output from the imager array is dependent upon the size and number of pixel elements in the imager array. High resolution pixel arrays have a slower read-out time due to the increased number of pixel elements. It is desirable to have a high resolution imager array (for slower read-out, radiographic mode) which may be operated in a low resolution mode (fluoroscopy mode) for faster read out of the signal representative of the detected image.

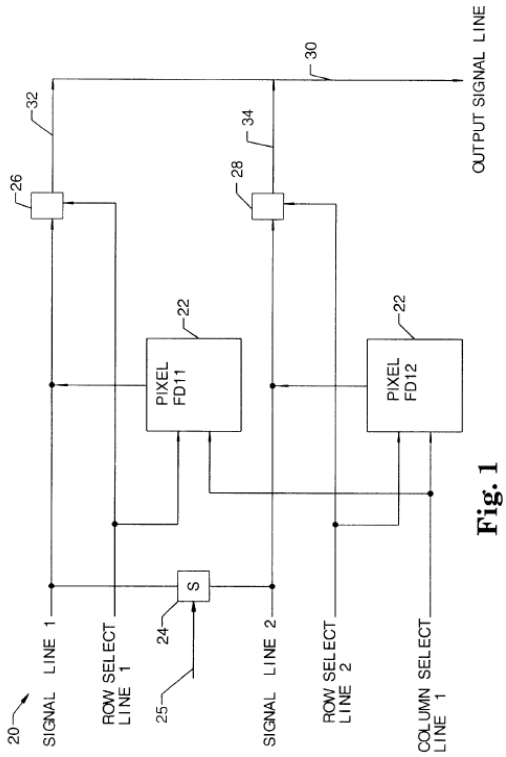

Fig. 1

Fig.5: An example of the pixel array which can be operated in high and low resolution modes

A pixel element 22 which provides an output signal representative of the intensity of the visible light detected. may be operated in a low resolution mode, wherein adjacent pixel element 22 are summed together to provide a faster read out of the image detected (Fig.5).

Pixel FD11 is electrically coupled to a signal line 1, and pixel FD12 is electrically coupled to a signal line 2. Signal line 1 is coupled to a buffer switch 26 , and signal line 2 is coupled to buffer switch 28. These buffer switches are included to provide isolated outputs to output signal line 30. Specifically, buffer switch 26 provides a buffered output signal 32 to output signal line 30, and buffer switch 28 provides a buffered output signal 34 to output signal line 30. When outputting simultaneously, the

buffered output signal 32 and buffered output signal 34 are summed onto the output signal line 30.

The pixel array can further include a row select line 1, a row select line 2, and a column select line 1. Row select line 1 is electrically coupled to pixel FD11 and buffer switch 26. Row select line 2 is electrically coupled to pixel FD12 and buffer switch 28. Column select line 1 is electrically coupled to pixel FD11 and pixel FD12.

In operation, when row select line 1 and column select line 1 are activated, the charge of pixel FD11 is read out to signal line 1. When row select line 1 is activated, buffer switch 26 is enabled for providing the buffered output signal 32, representative of the charge on pixel FD11, output to signal line 30. Similarly, when row select line 2 and column select line 1 are both activated, the charge of pixel FD12 is read out to signal line 2, and when row select line 2 is activated, buffered switch 28 provides on buffered output signal 34, representative of the charge on pixel FD12, output to signal line 30.

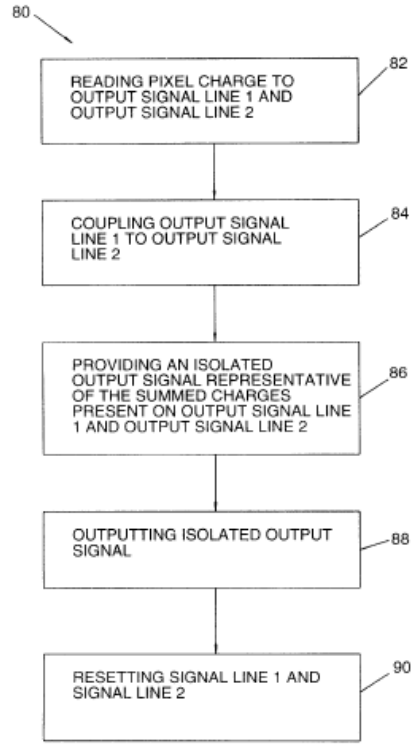

Fig. 6

Fig. 6: A method of reading out an imager in a low resolution mode with allows higher frame rates by binning (summing) the signal charge contained in an array of adjacent pixels.

Low resolution switch 24 may be activated to switch pixel array from a high resolution mode to a low resolution mode using a low resolution input signal 25. When low resolution switch 24 is activated, signal line 1 is coupled to signal line 2, and the charges present on signal line 1 and signal line 2 are summed together. When buffer switch 26 and buffer switch 28 are enabled, signal line 1 and signal line 2 operate in parallel, with the sum of buffered output signal 32 and buffered output signal 34 being present on output signal line 30. As such, pixel array operates in a low resolution mode with the signal present on output signal line 30 being representative of the sum of the two adjacent pixel elements, pixel FD11 and pixel FD 12, to provide a low resolution output signal having a fast read-out.

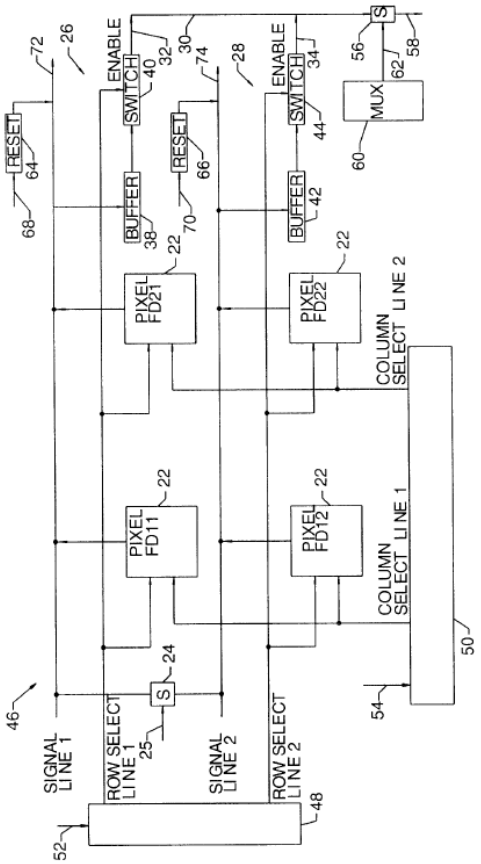

Fig.7: An example of the method of reading out in Fig. 6.

Referring to the flow diagram of Fig.6 and the exemplary embodiment of Fig.7, the method of summing adjacent pixel elements in a 2x2 pixel array includes reading the pixel charges of the 2x2 pixel array to their corresponding output signal line 1 and output signal line 2 (82). For summation of the charges on signal line 1 and signal line 2, signal line 1 is coupled to signal line 2 (84). An isolated output signal is provided which is representative of the summed charges present on signal line 1 and signal line 2 (86). The resulting isolated output signal is multiplexed with output signals from other pixel arrays for selectively outputting the output signal, such as to a memory device or for electrical display (88) in an imaging device. Once the

charges are read out, signal line 1 and signal line 2 are reset (90).

Referring to Fig. 8, in reading the pixel charge to output signal line 1 and output signal line 2, horizontal summation is accomplished by activating column select line 1 and column select line (92). Column select line 1 and column select line 2 is then activated by shifting or clocking adjacent ones through the horizontal shift register 50. The adjacent ones are shifted through the horizontal shift register 50 using two mutually exclusive phases of a single multi-phase clock signal 54 in Fig.7, as will be described in detail later herein.

Vertical summation can be accomplished by activating row select line 1 and row select line 2 (94). Row select line 1 and row select line 2 are activated by shifting or clocking adjacent ones through the vertical shift register 48. The adjacent ones are clocked through the vertical shift register 48 using two mutually exclusive phases of a single multi-phase clock signal 52.

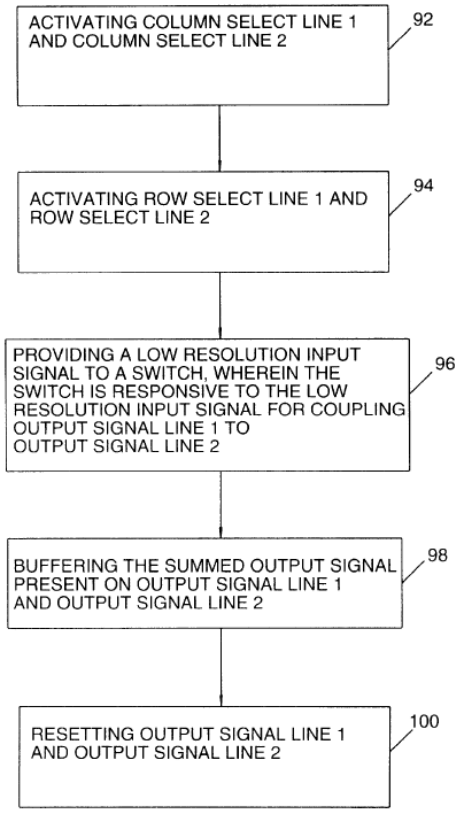

Fig.8: Another reading scheme.

Summation of the charged output to output signal line 1 and output signal line 2 are accomplished by coupling output signal line 1 to output signal line 2. Output signal line 1 is coupled by output signal line 2 by providing a low resolution input signal 25 to a switch 24 for coupling output signal line 1 to output signal line 2 (96).

The isolated output signal is output to the imaging device through a source follower transistor. As a preferred configuration, the output signal on signal line 1 and signal line 2 is output to output signal line 30 through isolation buffer 38 and isolation buffer 42 (98).. Output signal line 1 and output signal line 2 can be reset by providing a reset input signal to a reset switch for resetting output signal 1 and output signal line 2 to a referenced voltage (100).

IV. IMAGING PANEL

We have designed and built a module which facilitates attachment and detachment of the module relative to the base substrate and to a test fixture used in test and burn-in operations. The module is constructed to isolate the radiation detecting tile from thermal and/or mechanical stresses produced at the interconnections interface during attachment and detachment for test and burn-in, assembly and rework operations (Fig.10).

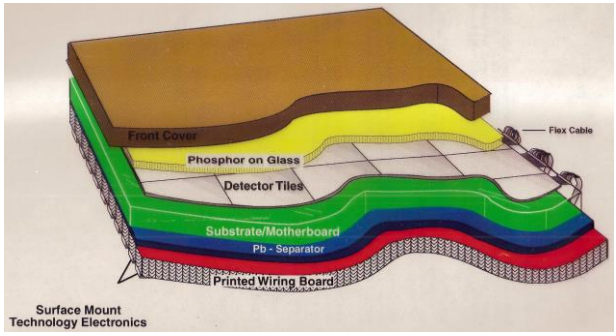

Fig.9. Cross sectional view of our indirect- type digital radiography detector which is based on the four-side buttable tiling scheme

With reference to Figs. 9 and 10, two sheets of glass – one is coated with a layer of phosphor and the other is mounted with a multitude of pixel arrays (tiles or modules) are bonded together to form a detector. The detector includes a base substrate and a plurality of radiation detecting modules mounted over the base substrate in an array. In the case of direct type (not shown), phosphor is not required and a thick layer of a-Se photoconductor (100-500 μm) is employed in place of photodiodes. Each of radiation detecting modules 14A includes a carrier substrate 16 and a radiation detecting tile 18 mounted over the carrier substrate. Each radiation detecting tile includes an array of radiation detecting elements (not shown) for detecting radiation on a pixel-by-pixel basis. Each of the radiation detecting elements can be realized , for example, by a photodiode, the combination of one or more transistors and one or more photodiodes, or the combination of a transistor disposed adjacent a photoconductor layer. If desired, a conventional or structured phosphor layer may be added to tile 18 or a

sheet of phosphor can be coated over a multitude of modules. . Each radiation detecting tile 18 is electrically coupled to conductive contacts on base substrate via conductive paths either provided by or associated with carrier substrate 16. In this manner, the electrical signals generated by the radiation detecting elements can be routed via base substrate to a digital acquisition system.

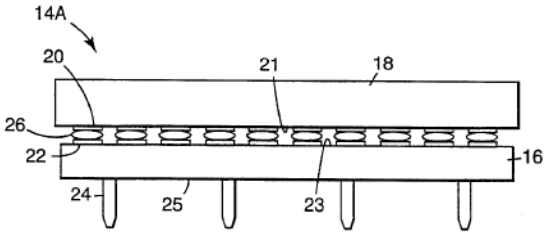

Fig. 10 illustrates a side view of an exemplary radiation detecting module useful in assembly of multi-module digital radiography detector.

As shown in Fig.10, module 14A includes carrier substrate 16 and radiation detecting tile 18. The radiation detecting tile 18 includes a plurality of electrically conductive contacts 20. Surface 23 of carrier substrate 16 may have an area sized slightly smaller than an area of surface 21 of radiation detecting tile. In other words, each of the major dimensions of surface 23 are smaller than the corresponding dimensions of surface 21. The carrier substrate would be sized slightly smaller than radiation detecting tile so that any registration error between the tile and the carrier substrate can be accommodated without interfering with subsequent alignment of modules on base substrate 12. Alternatively, surface of carrier substrate can be sized approximately equal to surface of radiation detecting tile provided that the sides of the carrier substrate are leveled such that surface 25 is smaller than surface 21. In addition, carrier substrate preferably has a coefficient expansion closely matched to that of radiation detecting tile to avoid stresses that could result from excessive heat during soldering and desoldering. The side edges of radiation detecting tile can be subjected to additional processing such as grinding, polishing, or beveling, as appropriate , to achieve desired gap dimensions, e.g., one to one-hundred microns, between adjacent tiles.

Contacts 20 and 22 comprise conductive contact pads and are are interconnected with solder balls 26. The surface tension of the solder balls in the molten state helps to align contact pads 20, 22 relative to another. The carrier substrate 16 includes internal conductive traces (not shown) that electrically couple contact pads 22 to conductive contacts 24 which are realized by tapered conductive pins. The pins 24 are configured to engage conductive sockets (not shown) formed in base substrate 12, providing both electrical and mechanical coupling of the module to base substrate. For testing and burn-in, pins 24 preferably are configured to removably engage conductive sockets formed in a test fixture. Thus, testing and burn-in operations can be performed with a reduced number of steps and little risk of damage to radiation detecting tile. This could help maintain device reliability despite rework operations, and can thereby reduce rework costs.

The internal conductive traces formed in carrier substrate can be accomplished with, for example, three layers of metallization. The metal layers can be patterned to form addressing lines, sensing lines, and DC current and provided with vias connecting contacts 22 and pins 24. A significant number of interconnections can be made internally within carrier substrate to electrically couple at least some of the contacts 20 via contacts 22 to common pins 24. Multiplexing circuitry can be incorporated within carrier substrate to help reduce the number of pins 24. In this manner, the number of interconnections between carrier substrate and base substrate can be greatly reduced, relative to the number of interconnections between the carrier substrate and radiation detecting tile. It is contemplated, for example, that the number of pins can be more than a factor of ten smaller than the number of contacts. Reduction in the number of pins can greatly facilitate attachment and detachment for test and burn-in, assembly, and rework operations.

V. EXPERIMENTAL RESULTS

A. Structured phosphor

Structured phosphor is employed to enhance image sharpness of the digital radiography detector since the emitted light is confined to the column with an area size equal to the photodetector size. Structured phosphors can be for example gadolinium oxysulfide doped with terbium (GdOS:Tb) or alkali halides doped with thallium (CsI:Tl) . CsI:Tl can be made in columnar structure by optimizing the evaporation conditions as shown in Fig.11 (a). Generally, for GdOS:Tb and CsI:Tl, columnar structure can be formed using the following approaches: (i) writing patterns on the phosphor using the laser (Fig.11b), (ii) creating mold using the microreplication technique (12a) and then filled with phosphor (Fig. 12b) or (iii) writing molds using a laser beam (Fig. 13 a and b)

B. Radiography Detector

A radiation detecting module of the size of 2.125”x2.125” was fabricated as shown in Fig. 14 (before phosphor coating) and Fig. 15 (after coating of a layer of GdOS:Tb phosphor). Each module has 624x624 pixels of a size of 85μm x 85μ, A multi-module (2x2) digital radiography detector is shown in Fig. 16.

VI. CONCLUSIONS

A four-side-buttable tiling scheme for a near real-time digital radiography detector is presented. The detector can be used in the field of medical imaging which includes fluoroscopic imaging and radiographic imaging. In fluoroscopic imaging, the imaging is read-out in a lower resolution mode; whereas in radiographic imaging, a high resolution read-out is desired. The multi-tile detector proposed in this paper is designed and built in such a manner that the number of interconnections between carrier substrate and base substrate can be greatly reduced, relative to the number of interconnections between the carrier substrate and radiation detecting tile. Consequently, the number of pins can be more than a factor of ten smaller than the number of contacts. Reduction in the number of pins can greatly facilitate attachment and detachment for test and burn-in, assembly, and rework operations.

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REFERENCES

[1] N.T.Tran and J.C.Dahlquist, "Solid state radiation detector", US 5,420,452

[2] N.T.Tran, N.W.Loeding and D.V.Nins, "Solid state electromagnetic radiation detector FET array", US 5,182,624

[3] N.T.Tran, "Process for producing a large area solid state radiation detector", US 5,254,480.

[4] N.T.Tran, "Radiation detector and fabrication method", US 5,942,756.

[5] N.T.Tran, Joseph Y. Pai and Choon-Woo Kim, "Solid state radiation detector having tiles photosensitive detectors arranged to minimize edge effects between tiles", US 5,545,899.

[6] N.T.Tran, Proceedings, 4th Annual Worlwide Scientific Conference, Information and Imaging Technologies Sector, 3M, Interlaken, Switzerland, October 14-19, 1990.

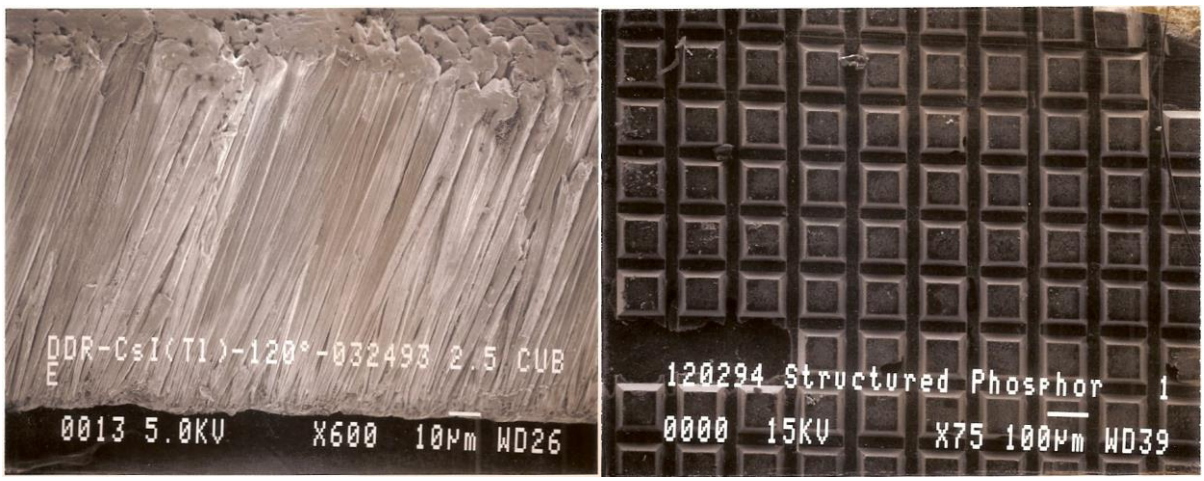

Fig. 11. (a) Evaporated (CsI :Tl) phosphor and (b) writing patterns on GsOS:Tb with a laser beam.

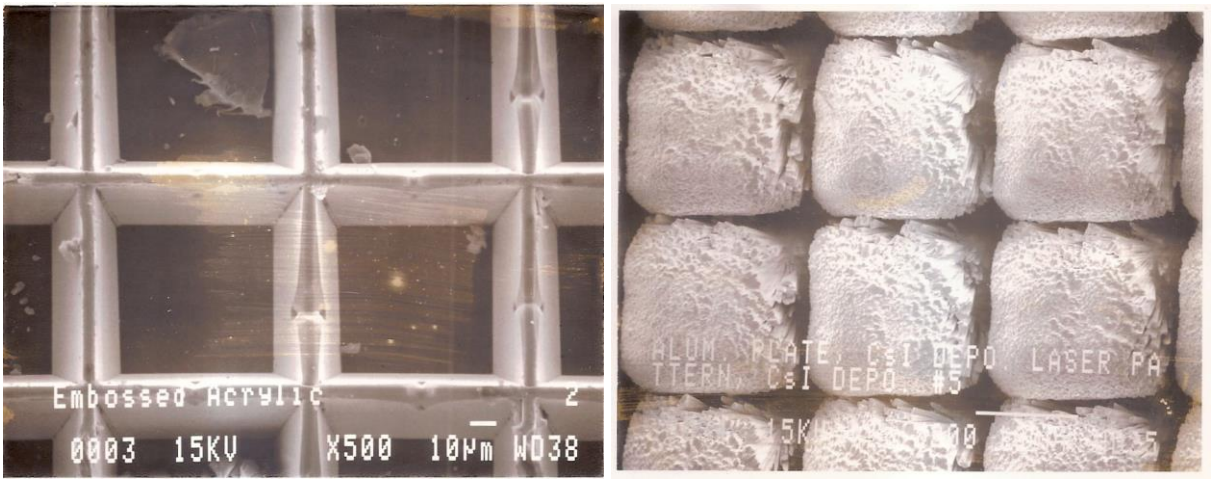

Fig. 12 (a) forming mold by microreplication and (b) filling the mold with CsI:Tl.

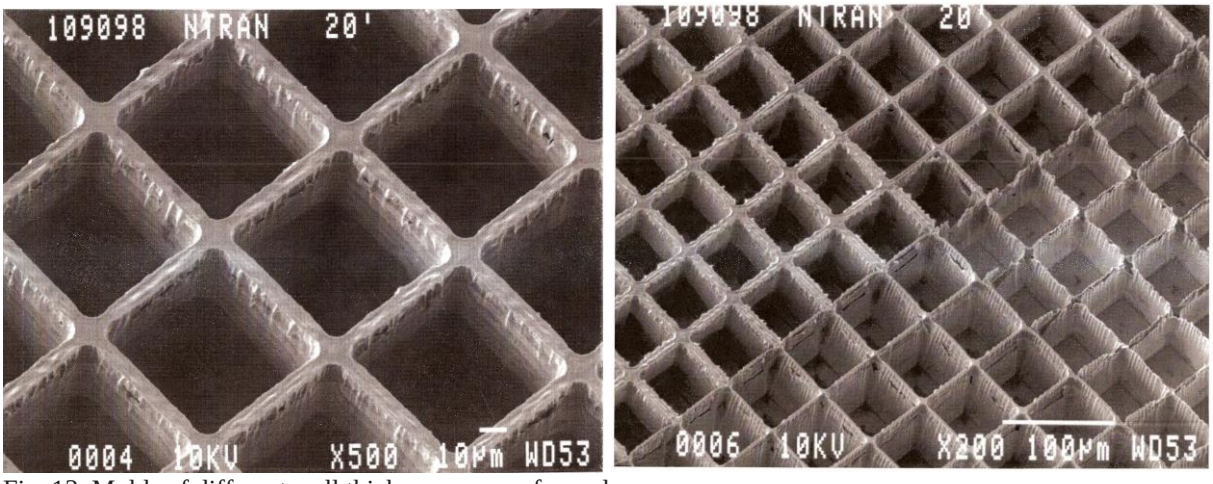

Fig. 13. Molds of different wall thicknesses were formed.

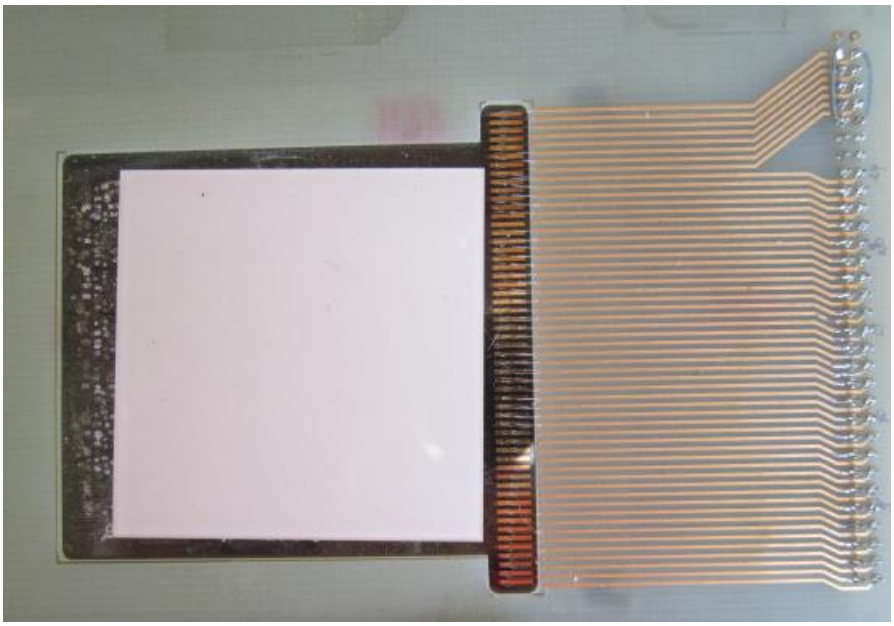

Fig. 14. Radiation detecting module a continuous layer of phosphor. Area = 2.125”x2.125”; pixel size= 85µm x85µm, 625x625 pixels

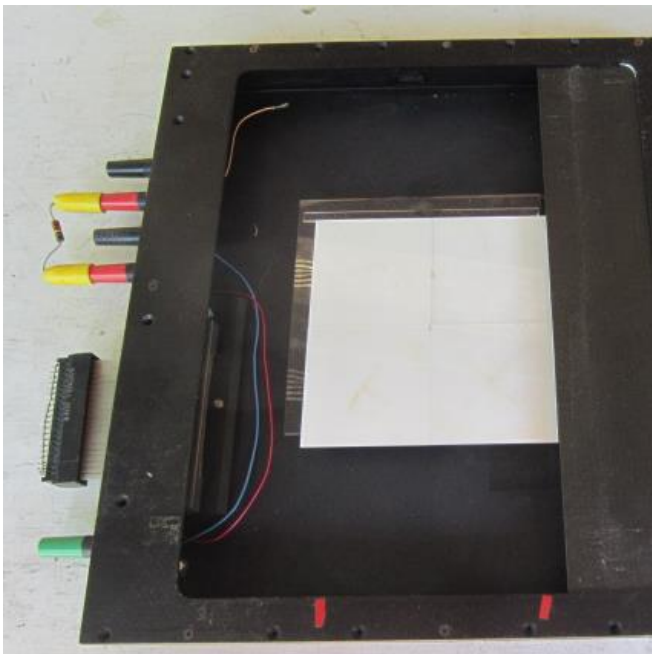

Fig. 15. Four modules of 2.125”x2.125” were tiled on a common substrate.